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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/682,957	11/02/2001	Andres Bryant	BUR920010071US1	3893

23123 7590 02/27/2004

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EXAMINER	
LEWIS, MONICA	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/682,957	BRYANT ET AL.	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed November 3, 2003.

Response to Arguments

2. Applicant's arguments with respect to claims 8-26 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 15 recites the limitation "the semiconductor layer." There is insufficient antecedent basis for this limitation in the claim.

5. Claims 23 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is meant by the following: a) "direct mechanical contact" (See Claims 23 and 26).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 8, 10-13, 14, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brigham et al. (U.S. Patent No. 6,380,010) in view of Houston (U.S. Patent No. 6,045,625).

In regards to claims 8 and 10-13, Brigham et al. ("Brigham") discloses the following:

a) a semiconductor wafer comprising a semiconductor layer (108) (For Example: See Figure 1);

b) a first recess and a second recess formed through the semiconductor layer (For Example: See Figure 2);

c) a body formed from the semiconductor layer situated between the first recess and the second recess, the body comprising a top body surface and a bottom body surface that defines a body thickness (For Example: See Figure 11);

d) a source structure (114) formed into the first recess, the source structure comprising a source region (For Example: See Figure 11);

e) a drain region (114) formed into the second recess, the drain structure comprising a drain region (For Example: See Figure 11); and

f) a top portion of the source structure and a top portion of the drain structure are within and abut the body thickness (For Example: See Figure 11).

In regards to claims 8 and 10-13, Brigham fails to disclose the following:

a) a semiconductor layer, that comprises single crystal silicon, overlying a buried insulator having three layers that comprise silicon dioxide, wherein the second layer comprises silicon nitride, wherein the third layer comprises silicon dioxide.

However, Houston discloses a semiconductor layer (16), that comprises single crystal silicon, overlying a buried insulator (14) having three layers that comprise silicon dioxide, and silicon nitride (For Example: See Figure 1, Figure 8c and Column 2 Lines 43-60). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Brigham to include a semiconductor layer, that comprises single crystal silicon, overlying a buried insulator having three layers that comprise silicon dioxide and

silicon nitride as disclosed in Houston because it aids in eliminating warping (For Example: See Column 1 Lines 49-62 and Column 2 Lines 43-60).

Additionally, since Brigham and Houston are both from the same field of endeavor, the purpose disclosed by Houston would have been recognized in the pertinent art of Brigham.

In regards to claim 14, Brigham discloses the following:

a) the body comprises a fin structure that comprises a top fin structure surface a bottom fin structure surface that define a fin structure thickness, wherein the top portion of the source structure and the top portion of the drain structure are below said top fin structure, and wherein said source structure and said drain structure abut the fin structure (For Example: See Figure 7).

In regards to claims 21 and 22, Brigham discloses the following:

a) a first and second recess (For Example: See Figure 1).

In regards to claims 21 and 22, Brigham fails to disclose the following:

a) a first portion of the buried insulator and a second portion of the buried insulator, and a third portion of the buried insulator.

However, Houston discloses a semiconductor with a semiconductor layer overlying a buried insulator having three layers (For Example: See Figure 1, Figure 8c and Column 2 Lines 43-60). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Brigham to include a semiconductor layer overlying a buried insulator having three layers as disclosed in Houston because it aids in eliminating warping (For Example: See Column 1 Lines 49-62 and Column 2 Lines 43-60).

Additionally, since Brigham and Houston are both from the same field of endeavor, the purpose disclosed by Houston would have been recognized in the pertinent art of Brigham.

8. Claims 9, 15, 18-20, 23-26, as far as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Brigham et al. (U.S. Patent No. 6,380,010) in view of Houston (U.S. Patent No. 6,045,625) and Zahurak et al. (U.S. Patent No. 6,593,192).

In regards to claim 9, Brigham fails to disclose the following:

a) the first layer of the buried insulator is at least as thick as the semiconductor layer.

However, Zahurak et al. ("Zahurak") discloses a buried insulator (20) that is at least as thick as the semiconductor layer (30) (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Brigham to include a buried insulator that is at least as thick as the semiconductor layer as disclosed in Zahurak because it aids in increasing performance (For Example: See Column 1 Lines 5-67 and Column 2 Lines 1-24).

Additionally, since Brigham and Zahurak are both from the same field of endeavor, the purpose disclosed by Zahurak would have been recognized in the pertinent art of Brigham.

In regards to claim 15, Brigham discloses the following:

a) a semiconductor wafer (For Example: See Figure 11);

b) a first recess and a second recess formed through the semiconductor layer (For Example: See Figure 11); and

c) a body formed from the semiconductor layer situated between the first recess and the second recess, the body comprising a top body surface and a bottom body surface that defines a body thickness (For Example: See Figure 11).

In regards to claim 15, Brigham fails to disclose the following:

a) a silicon layer buried on a buried insulator which comprises a first buried insulator on a second buried insulator different from the first buried insulator layer wherein the first buried insulator comprises silicon dioxide and the second buried insulator comprises a silicon nitride.

However, Houston discloses a semiconductor with a semiconductor layer, that comprises single crystal silicon, overlying a buried insulator having at least two layers that comprise silicon dioxide and silicon nitride (For Example: See Figure 1, Figure 8c and Column 2 Lines 43-60). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Brigham to include a semiconductor layer, that comprises single crystal silicon, overlying a buried insulator having at least two layers that comprise silicon dioxide and silicon nitride as disclosed in Houston because it aids in eliminating warping (For Example: See Column 1 Lines 49-62 and Column 2 Lines 43-60).

Additionally, since Brigham and Houston are both from the same field of endeavor, the purpose disclosed by Houston would have been recognized in the pertinent art of Brigham.

b) the first layer of the buried insulator is at least as thick as the semiconductor layer.

However, Zahurak discloses a buried insulator that is at least as thick as the semiconductor layer (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Brigham to include a buried insulator that is at least as thick as the semiconductor layer as disclosed in Zahurak because it aids in increasing performance (For Example: See Column 1 Lines 5-67 and Column 2 Lines 1-24).

Additionally, since Brigham and Zahurak are both from the same field of endeavor, the purpose disclosed by Zahurak would have been recognized in the pertinent art of Brigham.

In regards to claims 18-20, Brigham discloses the following:

a) the transistor comprises a source structure and a drain structure in said first recess and said second recess further comprises a fin structure (For Example: See Figure 11).

In regards to claims 23 and 26, Brigham fails to disclose the following:

a) the semiconductor layer is in direct mechanical contact with a gate dielectric layer at a surface of the gate dielectric layer, wherein the gate dielectric layer is in direct mechanical contact with a gate conductor layer, wherein the semiconductor layer is in direct mechanical contact with the buried insulator at a surface of the buried insulator, and wherein the surface of the gate dielectric layer is about parallel to the surface of the buried insulator.

However, Zahurak discloses a semiconductor layer (30) in direct contact with a gate dielectric layer (40) at a surface of the gate dielectric layer, wherein the gate dielectric layer is in direct contact with a gate conductor layer (42), wherein the semiconductor layer is in direct contact with the buried insulator (20) at a surface of the buried insulator, and wherein the surface of the gate dielectric layer is about parallel to the surface of the buried insulator (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Brigham to include a semiconductor layer in direct contact with a gate dielectric layer at a surface of the gate dielectric layer, wherein the gate dielectric layer is in direct contact with a gate conductor layer, wherein the semiconductor layer is in direct contact with the buried insulator at a surface of the buried insulator, and wherein the surface of the gate dielectric layer is about parallel to the surface of the buried insulator as disclosed in Zahurak because it aids in increasing performance (For Example: See Column 1 Lines 5-67 and Column 2 Lines 1-24).

Additionally, since Brigham and Zahurak are both from the same field of endeavor, the purpose disclosed by Zahurak would have been recognized in the pertinent art of Brigham.

In regards to claims 24 and 25, Brigham discloses the following:

a) a first and second recess (For Example: See Figure 1).

In regards to claims 24 and 25, Brigham fails to disclose the following:

a) a first portion of the buried insulator and a second portion of the buried insulator, and a third portion of the buried insulator.

However, Houston discloses a semiconductor layer overlying a buried insulator having three layers (For Example: See Figure 1, Figure 8c and Column 2 Lines 43-60). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Brigham to include a semiconductor layer overlying a buried insulator having three layers as disclosed in Houston because it aids in eliminating warping (For Example: See Column 1 Lines 49-62 and Column 2 Lines 43-60).

Additionally, since Brigham and Houston are both from the same field of endeavor, the purpose disclosed by Houston would have been recognized in the pertinent art of Brigham.

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brigham et al. (U.S. Patent No. 6,380,010) in view of Houston (U.S. Patent No. 6,045,625) and Choi (U.S. Patent No. 6,383,849).

In regards to claim 13, Brigham fails discloses the following:

a) a first recess and a second recess stop on a second layer of the buried insulator.

However, Choi discloses a semiconductor with a recess that stops on an insulator (For Example: See Figure 2e). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Brigham to include a recess that stops on an insulator as disclosed in Choi because it aids in improving the thermal conduction characteristics (For Example: See Column 2 Lines 15-43).

Additionally, since Brigham and Choi are both from the same field of endeavor, the purpose disclosed by Choi would have been recognized in the pertinent art of Brigham.

Conclusion

10. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) Burghartz et al. (U.S. Patent No. 5,461,250) discloses a SOI mosfet; b) Chau et al. (U.S. Publication No. 5,908,313) discloses a method of forming a transistor; c) Liang et al. (U.S. Patent No. 6,071,783) discloses a MOSFET; d) Yu (U.S. Patent No. 6,420,218) discloses a MOS transistor; and e) Xiang et al. (U.S. Patent No. 6,437,404) discloses a SOI device.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML
February 4, 2004

Mary Wilczewski
Primary Examiner